



AK2011 Datasheet

Version 1.0

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Revision History

Version	Date	Description
Ver1.0	May. 2008	1 st version released;

1 .Introduction

The AK2011 is a second generation single-chip highly-integrated digital music system solution for devices such as dedicated audio players. It includes an audio decoder with a high performance DSP with embedded RAM and ROM, USB interface for downloading music. AK2011 also provides an interface to flash memory, LED, button and switch inputs, headphones. Its programmable architecture supports WMA and other digital audio standards. For devices like USB-Disk, it can act as a USB mass storage slave device to personal computer system. The Chip has low power consumption to allow long battery life and an efficient flexible on-chip DC-DC converter that allows many different battery configurations, including 1xAA, 1xAAA and Li-ion. The built-in Sigma-Delta D/A includes a headphone driver to directly drive low impedance headphones. Thus, it provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital audio players.

Features:

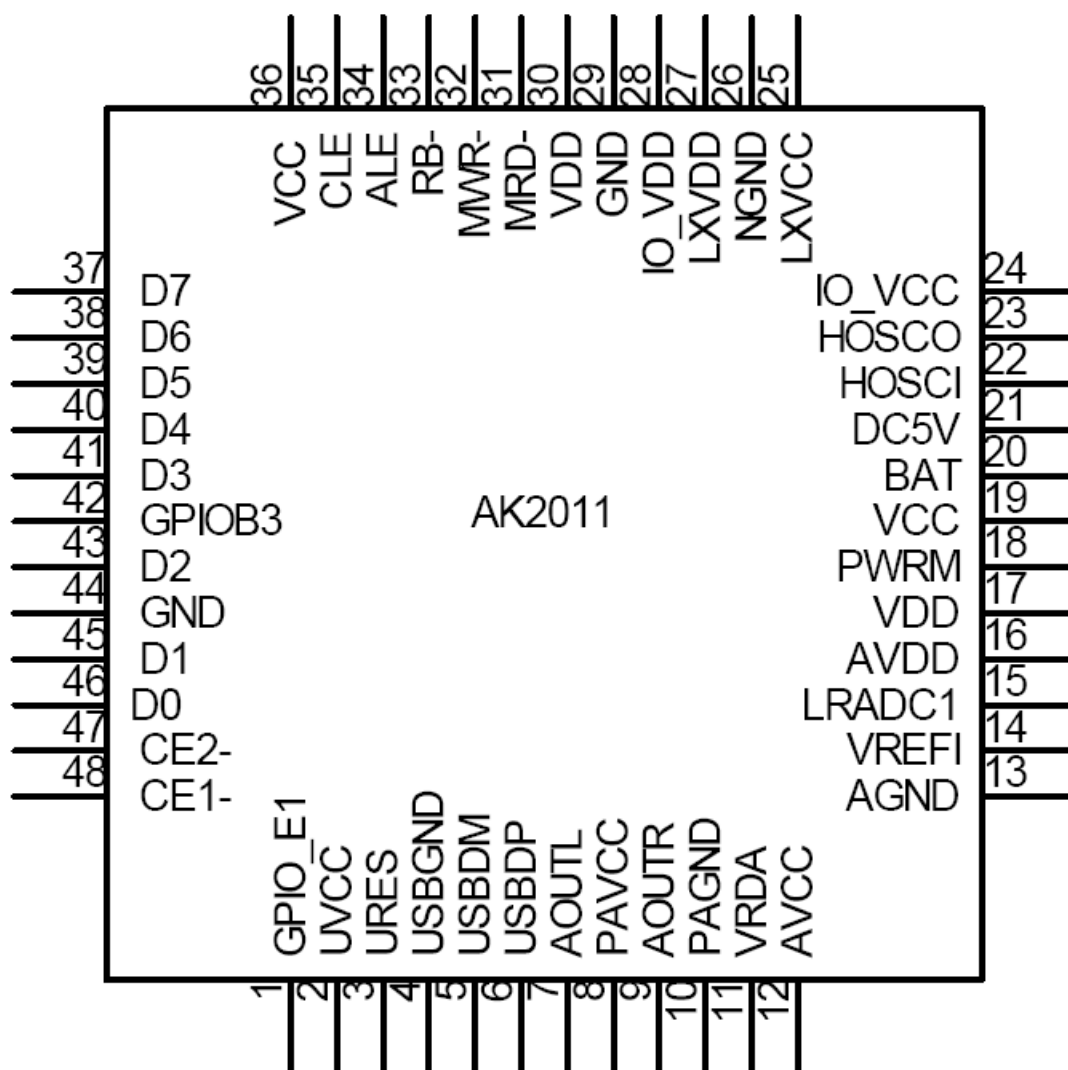
- MPEG1/2/2.5 Audio Layer 1,2,3 decoder, bit rate 8-448Kbps,8-48KHz,CBR/VBR
- Support WMA Decoder, bit rate 32-384Kbps,8-48KHz
- 24 bits DSP Core
- On-chip DSP PM with SRAM(16K*24) , can be switched to be MCU memory space
- On-chip DSP DM with SRAM(16K*24), can be switched to be MCU memory space
- Integrated MCU, the instruction set is compatible with Z80
- Internal ZRAM1((16K-64)*8),ZRAM2((12K+256)*8),ZRAM3(16K*8) accessed by MCU
- Internal 14Kx8 BROM build in Boot up and USB Upgrade firmware
- Internal (21K+12K)x8 TROM
- Internal SRAM access time<7ns, MROM access time<16ns
- External up to 2 (pcs) x 32M~4G bytes Nand type Flash accessed by MCU or DMA
- Support 24MHz OSC with on-chip PLL for DSP and about 32KHz RC oscillator
- 2-channel DMA, 1-channel CTC and interrupt controller for MCU
- Energy saving with dynamic power management, supporting 1 cell and Li-ion
- Support USB2.0 Compliance PHY+SIE, RD/WR:6MB/5MB (NAND Flash Base)
- Build in Stereo 21-bit Sigma-Delta D/A
- MCU runs at 48MHz (typ), F/W can program from DC up to 48MHz transparently
- DSP+PM/DM Speed up to 90MIPS, while 48mips@1.6v
- D/A+PA SNR: without A weight>91dB

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- Headphone driver output 2x20Mw @16ohm
- Standby Leakage Current: VCC:50uA@3.0V(MAX), VDD: [350uA@1.6V](#) (MAX)
- Low Power Consumption : <65mW@1.6V at typical MP3 decoder solution
<80mW@1.6V at typical WMA decoder solution

2. Pin Description

2.1 Pin Out



2.2 Pin Definition

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Pin No.	Pin Name	I/O Type	Driver	Reset Default	Description
1	GPIO_E1	BI	TBD2C	Z	Bit1 of General purpose I/O port E
2	UVCC	PWR	/	/	Power supply for USB
3	URES	AO	/	/	USB precision Resistor
4	USBGND	PWR	/	/	USB ground
5	USBDM	A	/	H	USB data minus
6	USBDP	A	/	H	USB data plus
7	AOUTL	AO	/	/	Int. PA left channel analog output
8	PAVCC	PWR	/	/	Power supply for power amplifier
9	AOUTR	AO	/	/	Int. PA right channel analog output
10	PAGND	PWR	/	/	Power amplifier ground
11	VRDA	AO	/	/	Bypass capacitor connect pin for Int. D/A Reference voltage
12	AVCC	PWR	/	/	power supply of Analog
13	AGND	PWR	/	/	Analog ground
14	VREFI	AI	/	/	Voltage reference input
15	LRADC1	AI	/	/	Low resolution A/D input 1
16	AVDD	PWR	/	/	Analog Core power pin
17	VDD	PWR	/	/	Digital Core power
18	PWRM	AI	/	/	POWER mode select
19	VCC	PWR	/	/	PAD power pin
20	BAT	I	/	/	Battery Voltage input.
21	DC5V	AI	/	/	5.0V Voltage
22	HOSCI	AI	/	/	High frequency crystal OSC input
23	HOSCO	AO	/	/	High frequency crystal OSC output
24	IO_VCC	PWR	/	/	IO for VCC DC-DC
25	LXVCC	PWR	/	/	VCC DC-DC pin
26	NGND	PWR	/	/	NMOS Ground
27	LXVDD	PWR	/	/	VDD DC-DC pin

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28	IO_VDD	PWR	/	Z	IO for VDD DC-DC
29	GND	PWR	/	/	Ground
30	VDD	PWR	/	/	Digital Core power
31	MRD-	O	NF_PAD	H	Ext. memory read strobe
32	MWR-	O	NF_PAD	H	Ext. memory write strobe
33	RB-	I	BD4C	H	Nand Type flash Ready/Busy status input.
34	ALE	O	NF_PAD	L	Address latch enable for NAND flash
35	CLE	O	NF_PAD	L	Command latch enable for NAND flash
36	VCC	PWR	/	/	PAD power pin
37	D7	BI	NF_PAD	L	Bit7 of ext. memory data bus
38	D6	BI	NF_PAD	L	Bit6 of ext. memory data bus
39	D5	BI	NF_PAD	L	Bit5 of ext. memory data bus
40	D4	BI	NF_PAD	L	Bit4 of ext. memory data bus
41	D3	BI	NF_PAD	L	Bit3 of ext. memory data bus
42	GPIO_B3	BI	BD2XM5	Z	Bit3 of General purpose I/O port B
43	D2	BI	NF_PAD	L	Bit2 of ext. memory data bus
44	GND	PWR	/	/	Ground
45	D1	BI	NF_PAD	L	Bit1 of ext. memory data bus
46	D0	BI	NF_PAD	L	Bit0 of ext. memory data bus
47	CE2-	O	NF_PAD	H	Ext. memory chip enable 2
	GPIO_A4	BI		/	Bit4 of General purpose I/O port A.
48	CE1-	O	NF_PAD	H	Ext. memory chip enable 1

NOTE:

- 1: PWR—Power Supply
- 2: AI—Analog Input
- 3: AO—Analog Output
- 4: O—Output
- 5: I—Input
- 6: BI—Bidirection
- 7: TBD2C, BD2C, BD2XU, SBD2X, BD2XM5—2 miliampere driver
- 8: BD4CM2, BD4C, BD4CU—4 miliampere driver

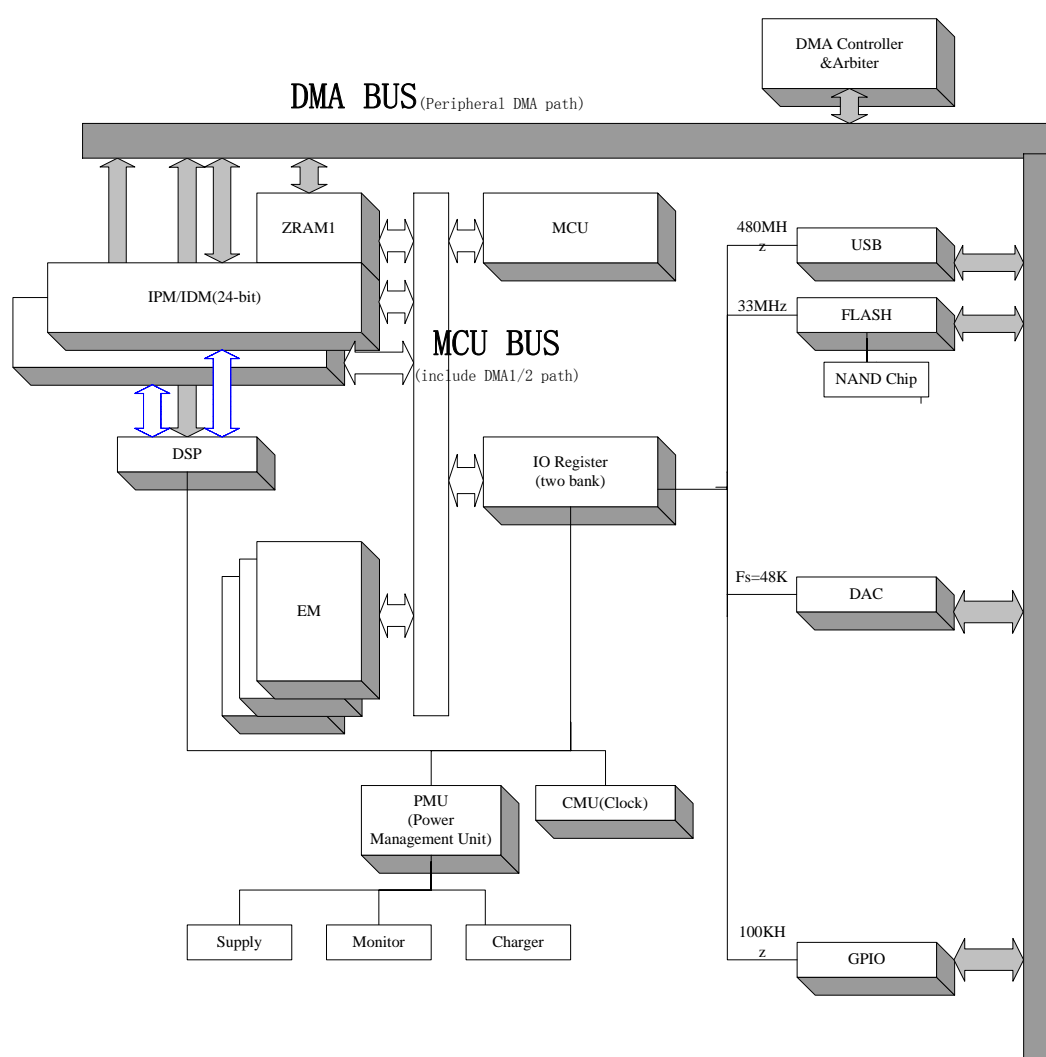
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9: BD1XM2—1 miliampere driver

10: USCU—USCHIMITCU

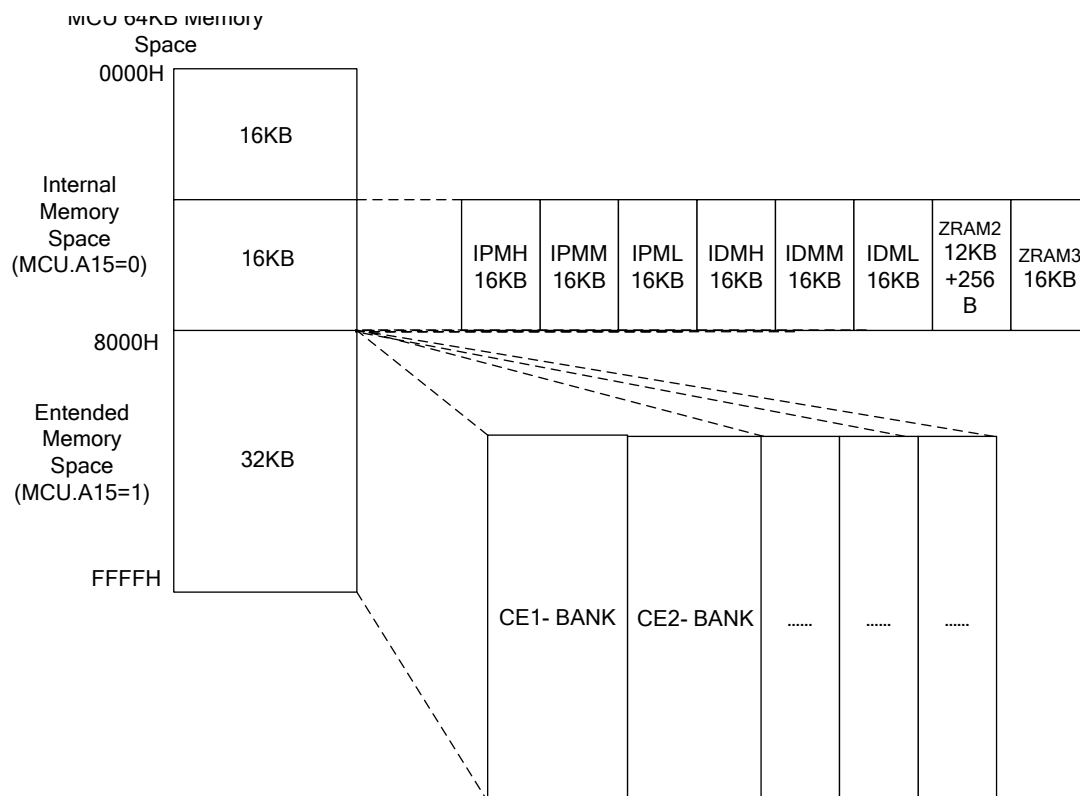
3. Function Description

3.1 Functional Block Diagram



3.2 MCU Core

3.2.1 MCU System Memory Mapping



If IA15=0 -> mapped to internal Memory

If IA14=0, mapped to internal ZRAM (16K-64 ZRAM1)

If IA14=1, mapped to internal DSP IPM/IDM when they are mapped into MCU memory space. 3 extended address bits of an IO mapped register (Mapped at Register) are used to decode the access to one of these memory blocks

Bit 2 1 0	Accessed Block
0 0 0	IPM low byte
0 0 1	IPM middle byte
0 1 0	IPM high byte
0 1 1	ZRAM3
1 0 0	IDM low byte
1 0 1	IDM middle byte
1 1 0	IDM high byte

1 1 1 ZRAM2 (B1+B2+URAM)

Since IPM/IDM is mapped to MCU memory space per 8K block, IA13 is used to select low/high block of 8K bytes in each 16K byte block.

If IA15=1 -> Extended address bits are IO mapped at 01h and 02h for EMA15-25.

EMA15-21 are address bus, while the EMA23-25 are used to decode CEs.

CE0- is used to access boot code from ROM/MASK/NOR- type Flash

CE1- to CE2- can be configured to access ROM, or RAM or NAND-type Flash

Internal MCU MROM/SRAM memory mapping:

- 1) (16K-64)byte ZRAM1(IA15=0,IA14=0) : 0000H-3FBFH
- 2) 8Kbyte B1+B2(IA15=0,IA14=1,IOReg05.[2:0]=111): 4000H-5FFFH
- 3) (4K+256) byte URAM: 6000H-70FFH, it has synchronization and asynchronism accessing modes.
- 4) 16Kbyte ZRAM3(IA15=0,IA14=1,IOReg05.[2:0]=011): 4000H-7FFFH
- 5) 14Kbyte BROM(IA15=1,Reg02=00h, Reg01=00h) : 8000h-B7FFh
- 6) 21Kbyte TROM1(IA15=1,Reg02=00h,Reg01=02h) : 8000h-D3FFh
- 7) 12Kbyte TROM2(IA15=1,Reg02=00h,Reg01=03h) : 8000h-AFFFh

Internal DSP IPM/IDM memory mapping:

- 1) 16K x24bit IPM SRAM : 0000H-3FFFH
- 2) 16K x24bit IDM SRAM : 0000H-3FFFH

Internal DSP IPM/IDM memory mapping accessed by MCU:

- 1) 16K x3 byte IPM SRAM : 4000H-7FFFH
- 2) 16K x3 byte IDM SRAM : 4000H-7FFFH

(Hi/Mid/Low Byte Select and Mapping Mode controlled by IOReg05)

DMA MODE NOTE:

- 1: When DMA1 and DMA2 are active, MCU will halt, while DMA1 and DMA2 have priority.
- 2: CARD DMA, FLASH DMA or USB DMA is active, MCU will not halt.

3.3 DSP24 Core

This Core is a high performance, programmable Digital Signal Processor (DSP) suitable for a variety of digital audio compounding functions, such as Dolby AC-3 Surround, MPEG1 Layer3 which require large memory provided and the higher accuracy. RDSP24 is a general purpose DSP which can be appended various peripherals circuitry to implement some advanced signal processing algorithms for audio application.

3.4 ZRAM1, ZRAM2 & ZRAM3

Speed: max read time 30 ns from ZRAMRD- going low

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

ZRAM2 is composed of B1, B2 and URAM: 4K+4K+(4K+256). All of them can be operated independently. It has the following modes:

- 1) MCU running at ZRAM1, while DMA[M] read B1 and DMA[N] write B2. Vise versa.
M=4,5,6; N=4,5,6; M!=N.
- 2) MCU is running at ZRAM1, while DMA[M] read B2 and DMA[N] write ZRAM3. Vise versa.
M=4,5; N=4,5; M!=N.
- 3) MCU is running at ZRAM1, while DMA[M] read B1 and DMA[N] write ZRAM3. Vise versa.
M=4,5; N=4,5; M!=N.
- 4) MCU running at ZRAM1 or ZRAM2 or ZRAM3.

IPM and IDM

Power consumption: stand by when both WR- and RD- are inactive, access current as low as possible.

PM/DM can be accessed by MCU, DSP, DMA1, DMA2, DMA4 and DMA5.

When DSP is accessing the high (low) 8Kbytes, MCU/DMA1, 2, 4, 5 can access low (high) 8K bytes at the same time.

3.5 USB2.0 SIE

3.5.1 General Description

The Artek USB2.0 device controller is fully compliant with the Universal Serial Bus 2.0 specification. In high-speed mode this device is capable of transmitting or receiving data up to 480Mbps. This high performance USB2.0 device controller integrates USB transceiver, SIE, and provides multifarious interfaces for generic MCU, RAM, ROM and DMA controller. So it is suitable for a variety of peripherals, such as: scanners, printers, mass storage devices, and digital cameras. It is designed to be a cost-effective USB total solution.

3.5.2 Features

- Fully compliant with USB Specification 2.0

- Supports USB High Speed (480Mb/s) and Full Speed (12Mb/s)
- Supports Control, Bulk, Isochronous and Interrupt Transfers
- Embedded USB high-speed Transceiver which complies with Inter UTMI
- Supports DMA interface (16-bit)
- 2K bytes configurable FIFO for endpoints and provides double buffer to increase throughput.
- Supports USB remote wake-up feature
- Software controlled connection to USB bus for re-enumeration

3.6 NAND Flash

The NAND Flash is a configurable interface to external NAND Flash. The highly configurable and flexible interface can attach to using most of readily available NAND Flash device. The flash data bus can be configured to be 8-bit access.

The controller automatically generates the Reading, Programming and Other commands timing by proper CLE, ALE and CE controls. So reliable data transferring between the Int. RAM and ext. Flash by MCU or DMA is available.

3.7 General Purpose IO Ports

AK2011 has GPIOA, GPIOB and GPIOE. They have different functions in different modes.

GPIO	F1(CE0S=H default)
GPIO_A4	CE2-/GPIO_A4
GPIO_B3	GPIO_B3 (10mA)
GPIO_E1	GPIO_E1

3.8 HOSC/PLL

AK2011 supports 24Mhz crystal which is the system clock source.

A low jitter PLL referenced to 24MHz is used to generate clock for DSP and for serial communication protocols such as USB. The clock used in serial communications

is 48MHz. Another PLL referenced to 24MHz is used to generate 22.5792MHz for sample rate 44.1K/22.05KHz/11.025KHz and 24.576MHz for audio sequence of 48Khz.

3.9 PMU

3.9.1 DC-DC Converters & Regulators

There are two on-chip DC-DC converters and two Regulators. DC-DC2 converter can work in Buck and Boost mode for different input voltage, while DC-DC1 can only work in Boost Mode. Both of these two DC-DC converters work in PFM or PWM modulation for different load current.

Power mode configuration

PWRM	DC5V>4.3V	DC-DC1	Regulator1	DC-DC2	IO_VDD	Regulator2	Description
0	0	Boost	N	Boost	VDD	N	1 Alkaline/NIMH, 2 Inductor
0	0	Boost	N	N	GND	From VCC	1 Alkaline/NIMH, 1 Inductor
1	0	N	Y	Buck	BAT	N	Li+, 1 Inductor
X	1	N	Y	N	-	From VCC	USB

3.9.2 Battery Monitor

There is a low speed 6-bit A/D for Battery monitor and wire control.

The relationship between battery type and the A/D input range is:

Relationship between Battery Type and A/D Input Range

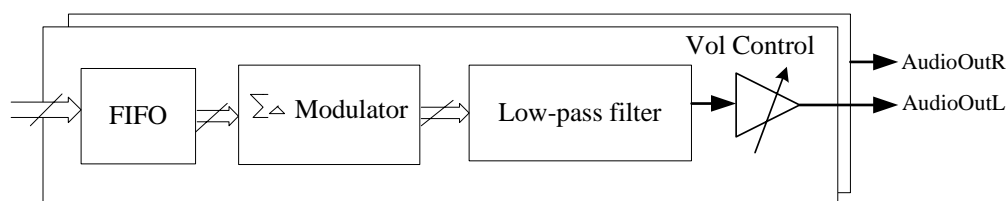
Battery type	Internal Voltage divider for battery	Input range
1 Alkaline/NIMH	1	0.7~2.2V
1 Li+	1/3	0.7~2.2V

3.10 D/A and Headphone Driver

3.10.1 D/A Interface

AK2011's internal D/A is an on-chip Sigma-Delta Modulator, a high performance D/A is composed of it and the D/A analog block referenced to 17.2. The D/A interface support 4-level play back FIFO (8 X 20-bit PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256XFS clock for over-sampling, while 24.576MHz supports 48K/32K/24K/16K/12K/8KHz with 256XFS for over-sampling.

D/A Block Diagram



Internal D/A can drive earphone directly and the pin PAVCC need a bypass capacitor about 100uF to eliminate the “PENG” when D/A is powered on or off. D/A includes an analog mixer, reference to the ADDA block diagram.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Typical	Rating	Unit
Supply voltage	VDD	1.6	-0.3~2.0	V
	VCC	3.0	-0.3~3.6	V
Input voltage	V _I		-0.3~3.6	V
Storage temperature	T _{stg}	25	-65~150	°C

Note:

1. T₀ = 25°C (Operating Temperature)
2. Do not short-circuit two or more output pins simultaneously.
3. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

4.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C _I	f _c = 1 MHz		15	pF
I/O capacitance	C _{IO}	Unmeasured pins returned to 0 V		15	pF

Note: T₀ = 25°C, VCC = 0 V.

4.3 DC Characteristics

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Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	$I_{OH} = -6 \text{ mA}$	2.4			V
Low-level output voltage	V_{OL}	$I_{OL} = 6 \text{ mA}$			0.4	V
High-level input voltage	V_{IH}		$0.6 \cdot V_{CC}$		$V_{CC} + 0.6$	V
Low-level input voltage	V_{IL}		-0.3		$0.4 \cdot V_{CC}$	V
Input leakage current	I_{LI}	$V_{CC} = 3.6 \text{ V}, V_I = V_{CC}, 0 \text{ V}$			± 5	μA
Tri-State leakage current	I_{LO}	$V_{CC} = 3.6 \text{ V}, V_I = V_{CC}, 0 \text{ V}$			± 3	μA
GPIO Drive	I_{drive3}	GPIO_A4		6		mA
		GPIO_B3		16		
		GPIO_E1		6		

NOTES:

- $T_o = -10 \text{ to } +70^\circ\text{C}$, $V_{DD} = 1.6 \text{ V}$, $V_{CC} = 3.0 \text{ V}$

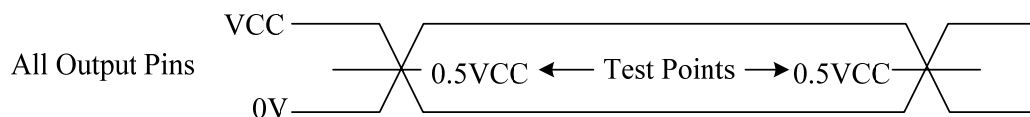
4.4 A C Characteristics

$T_o = -10 \text{ to } +70^\circ\text{C}$

4.4.1 AC Test Input Waveform

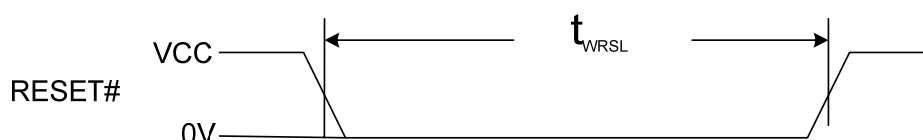


4.4.2 AC Test Output Measuring Points



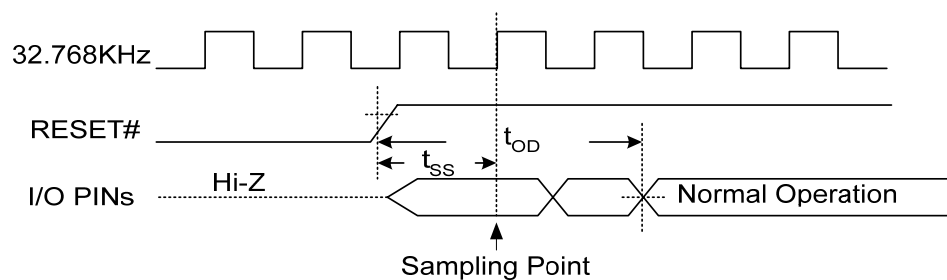
4.4.3 Reset Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	50	—	us



4.4.4 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{ss}		—	61.04	us
Output delay time (from RESET#)	t_{OD}		61.04	—	us



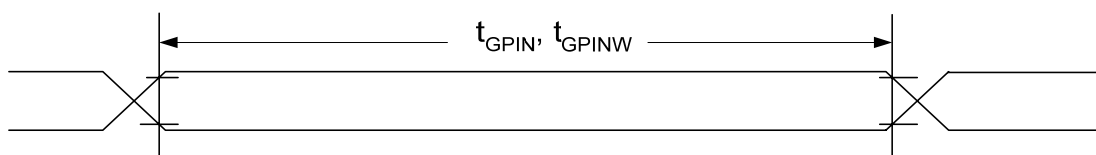
4.4.5 GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIIN}	Normal operation	$11/f_{mcucclk}$		s
GPIO output rise time	t_{GPRISE}		5	50	ns

GPIO output fall time	t_{GPFALL}		5	50	ns
Output level width	t_{GPOUT}		$11/f_{mcuclk}$		s

Notes 1. f_{MCUCLK} is the frequency that MCU is running upon.

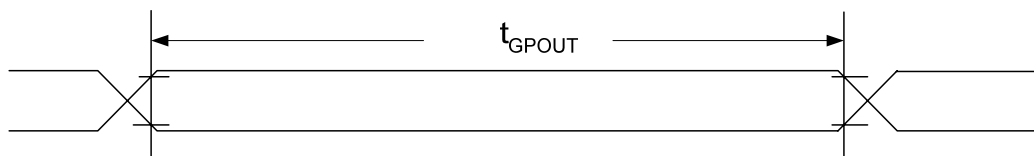
Input level width



Output rise/fall time



Output level width

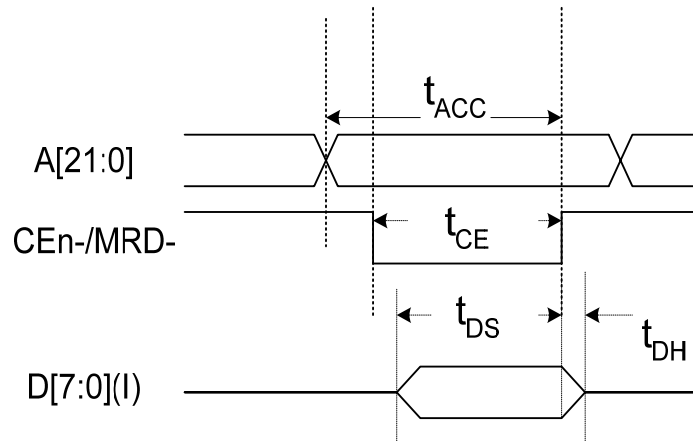


4.4.6 Ordinary ROM Parameter

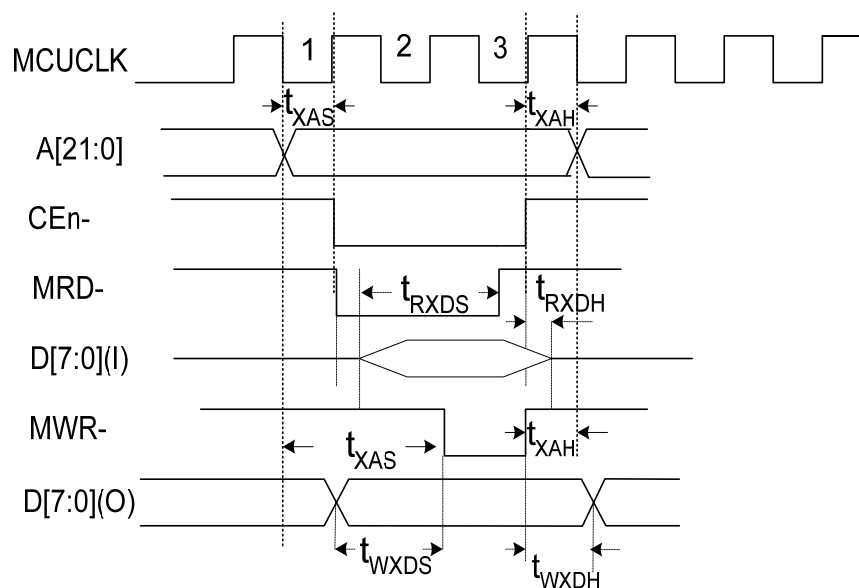
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address) ^{Note}	t_{ACC}	HOSC=24MHz	90		ns
Data access time (from CEx#) ^{Note}	t_{CE}	HOSC=24MHz	90		ns

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Data input setup time	t_{DS}	HOSC=24MHz	40		ns
Data input hold time	t_{DH}	HOSC=24MHz	15		ns



4.4.7 External System Bus Parameter



Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal) ^{Note 1, 2}	t_{XAS}	Memory Read	10		ns

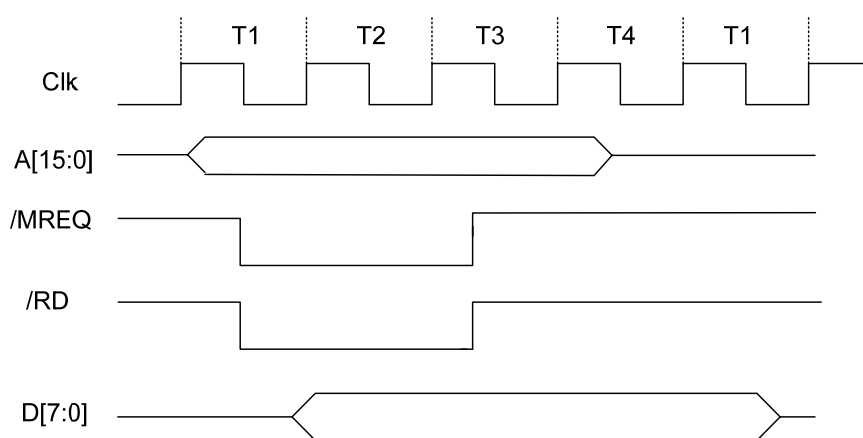
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal) ^{Note 1, 2}	t_{XAH}		5		ns
Data output setup time (to command signal) ^{Note 1}	t_{WXDS}		20		ns
Data output hold time(from command signal) ^{Note 1}	t_{WXDH}		10		ns
Data input setup time (to command signal) ^{Note 1}	t_{RXDS}		20		ns
Data input hold time (from command signal) ^{Note 1}	t_{RXDH}		10		ns

Notes: 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. $T \text{ (ns)} = 1 / f_{MCUCLK}$

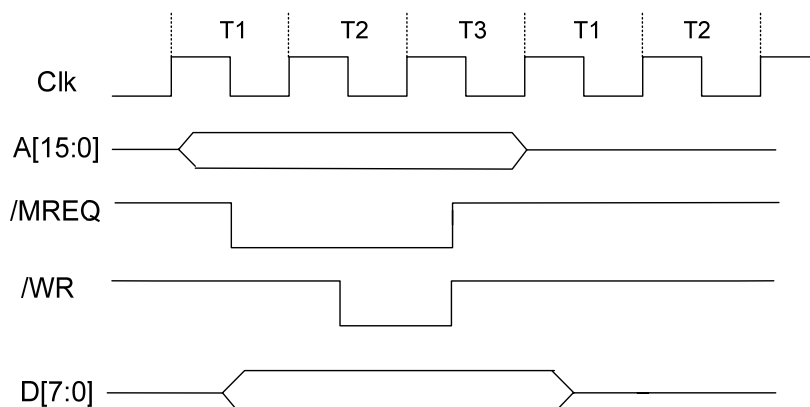
4.4.8 Bus Operation

Memory Read Timing



Memory Read Timing

Memory Write Timing



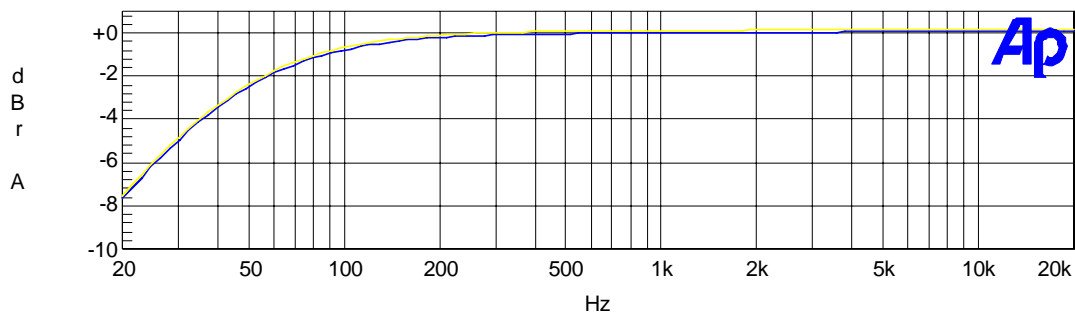
Memory Write Timing

4.4.9 Headphone Driver Characteristics Table

($T_o = -10 - +70^{\circ}\text{C}$, $V_{DD} = 1.6\text{ V}$, $V_{CC} = 3.0\text{ V}$, Sample Rate=32KHz, Volume Level=0x1F)

Characteristics	Min	Typ	Max	Unit
Dynamic Range -60 dBFS Input		-87		dB
Total Harmonic Distortion + Noise		-81		dB
Frequency Response 20-20KHz	-7.6	0		dB
Output Common Mode Voltage		1.5		V
Full Scale Output Voltage		1.3		V _{pp}
Inter channel Gain Mismatch(1KHz)		-66		dB

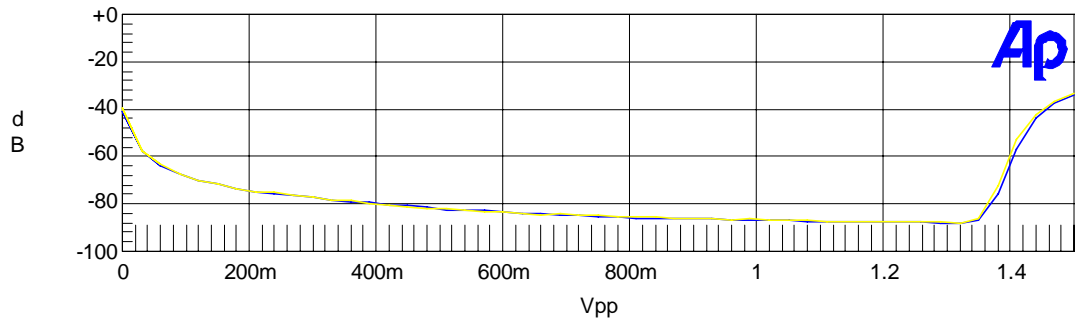
Frequency Response Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.Level A	Left	
1	3	Yellow	Solid	1	Anlr.Level B	Left	

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THD + N Amplitude Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Blue	Solid	1	Anlr.THd+N Ratio	Left	
1	2	Yellow	Solid	1	Anlr.THd+N Ratio	Left	

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5. Ordering Information

5.1 Soldering Conditions

Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions
Infrared ray reflow	Peak package's surface temperature: 235℃(Lead) or 260℃(Lead Free)
	Reflow time: 30 seconds or less (210℃ or more)—(Lead) or 60 seconds or less (217℃ or more)— (Lead Free)
	Maximum allowable number of reflow processes: 2
	Exposure limit: 1 days at Rh=60%, Tem=30℃ (12 hours of pre-baking is required at 125℃ afterward).
Partial heating method	Terminal temperature: 300℃ or less
	Heat time: 3 seconds or less (for one side of a device)

Note: Maximum number of days during which the product can be stored at a temperature of 25℃ and a relative humidity of 65% or less after dry-pack package is opened.

Caution: Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

5.2 Precaution against ESD for Semiconductors

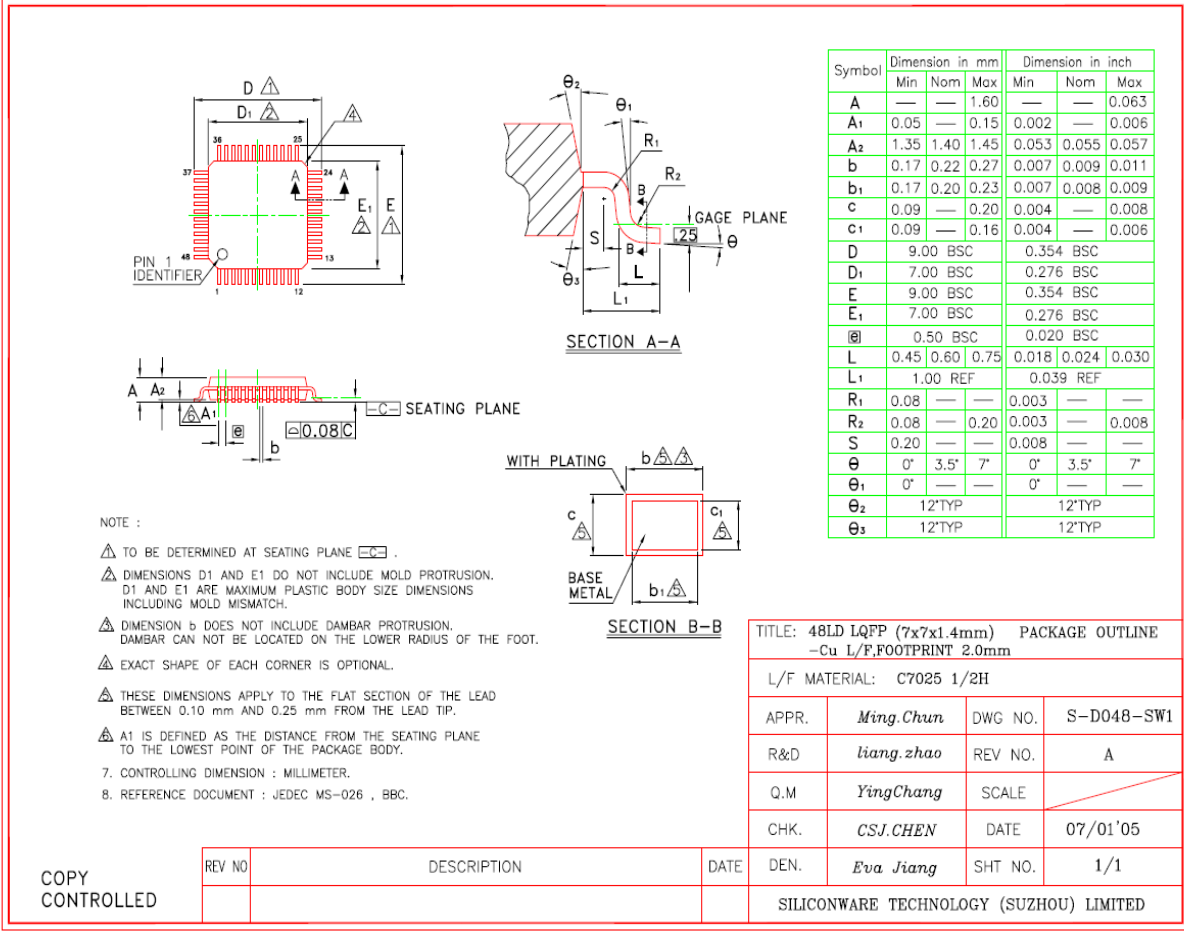
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

5.3 Status before Initialization of MOS Devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is

not initialized until the reset signal is received. Reset operation must be executed immediately after power-on.

6. AK2011 Package Drawing



7 Acronym and Abbreviations

ACK—Acknowledgement

ADC—Analog Digital Convert

CTC—Clock/Timer/Counter

DAC—Digital Analog Convert

DMA—Direct Memory Address

DRQ—Data Request

DST—Destination

ECC—Error Correction Code

EM—External Memory

FIFO—First In First Out

HIP—Host Interface Port

HOSC—High Frequency Oscillator

IDM—Internal Data Memory

IPM—Internal Program Memory

IRQ—Interrupt Request

LOSC—Low Frequency Oscillator

NAK—Negative Acknowledgement

PLL—Phase Locked Loop

RTC—Real Time Clock

RB—Ready/Busy

SRC—Source